25.6 A Blocker-Vigilant Channel-Select Filter with Adaptive IIP3 and Power Dissipation

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One reason for the large power dissipation of channel-select filters is that they have to be designed with high linearity in case a large blocker is present at the input. However, this large power dissipation is unnecessary when such blockers are absent or are of reduced strength, which is often the case [1]. This paper discusses a technique for drawing supply current only as required by the magnitude of the blockers, thus keeping the average power dissipation low. In contrast to earlier work [2, 3], here we sense only the blocker level, and provide a fully integrated solution, including all supporting circuitry.

The technique is applied to opamp *RC* leapfrog filters. The opamps in the first two stages use Class-AB outputs. A low standby current is enough to provide satisfactory linearity at signal frequencies because of the large loop gain at such frequencies. At blocker frequencies, though, the loop gain is low and, if a blocker is present, significant nonlinearity can result; therefore, the bias current needs to be increased to keep such nonlinearity in check. This is accomplished as shown in Fig. 25.6.1. A level-detecting circuit is provided in the first two stages, where large blocker levels are anticipated. The use of a local dynamic biasing loop facilitates a fast response to the appearance of blockers. The opamp input is not a "virtual short" at high frequencies, since this input (V_x in Fig. 25.6.1) is $V_{out}/A(f)$ and, for a given output level, its magnitude increases at higher frequencies as $|A(f)|$ decreases. The gains from V_{IN} to V_{OUT}, and from V_{IN} to V_X are shown versus frequency in Fig. 25.6.1. Typical amplitudes of V_X when a blocker is present are in the tens of mV. In the control loop shown, the level detector circuit compares the envelope of V_X with a reference voltage, and feeds a bias control signal back to the opamp, thus adjusting the open-loop gain of the opamp, $|A(f)|$, by controlling its transconductance. This is possible since the open-loop gain of a properly designed two-stage opamp can be, at the frequency of interest, expressed by

$$A(s) \approx \frac{g_m}{sC_c} \quad (1)$$

where g_m is the transconductance of the first stage and C_c is the frequency compensation capacitor.

Fig. 25.6.2 shows the schematic diagram of the fully differential opamp employed as the first and second opamps in Fig. 25.6.1. The current mirror comprising M_1 and M_2 provides a quiescent current I_0 (10μA) to the opamp; the cascode PMOS transistors M_3 and M_4 provide an extra control current I_{CNT} (0 to 150μA) through V_{CNT}. The sum $I_o + I_{CNT}$ flows into the input differential pair and the two differential pairs used for the common-mode feedback. The change of the bias current propagates towards the output stage through the class-AB bias circuit [4]. The proportional current increase in each gain stage ensures stability. A modified cascoded Miller compensation scheme is introduced to avoid an unacceptable departure of the optimal compensation point as the bias currents increase. The use of a class-AB output stage corresponds to a form of agile dynamic biasing and is useful in the case of abrupt large blocker input changes, in contrast to a class-A bias output with an insufficient bias current, which could cause a diminution of the desired signal when the blocker level exceeds a certain limit. In the downstream stages of the filter, where the blockers are significantly attenuated, simple opamp circuits are used, with minimal class-A bias, as the bias current is not compromised in any case.

The level detector circuit is shown in Fig. 25.6.3. The preamplifier amplifies V_X to a level at which the subsequent peak detector [5] can efficiently operate. The PMOS transistors used in the peak detector are biased in weak inversion, which is sufficient for envelope detection. Because the peak detector used has a large sensitivity to the common-mode signal, the preamplifier also works as a common-mode rejector. Input capacitors block the dc component that arises in the opamp, which could otherwise cause a detection error at the peak detector. Dynamic biasing in the low-pass filter following the detector ensures a fast ramp-up when a large blocker appears, in spite of the fact that this filter is inherently slow due to the low cut-off frequency needed for the envelope detection.

A 5th-order Butterworth low-pass filter has been implemented using a UMC 0.18μm CMOS process with a 1.8V supply voltage. The active area occupies 0.38mm^2. A chip micrograph is shown in Fig. 25.6.7. Figure 25.6.4 shows the transient behavior of the filter. The plots on the left show the situation when a 1MHz, -43dBV (-30dBm in 50Ω) in-band signal is present, and a 10MHz, -18dBV blocker appears at the input; as seen, the blocker is effectively eliminated at the output without disturbing the response to the signal, apart from a change in dc offset. The plots on the right show the situation when two -18dBV blockers, at 10MHz and 21MHz, appear at the input, the output is shown with the dynamic biasing OFF and with it ON; in the latter case the IM3 component at 1MHz effectively disappears without causing significant transients.

Figure 25.6.5 shows the IM3 output component, the input 3rd-order intercept point for out-of-channel blockers, and the total supply current, with two blockers present at the input at 10 and 21MHz, versus the level of the blockers, with the measured IM3 at 1MHz. The attainable IIP3 level is variable by adjusting the reference voltage, V_{REF}, in Fig. 25.6.3. The quiescent currents of the 5th-order filter and two detectors are 1.2mA and 60μA, respectively. The input-referred in-band integrated noise is about 140μV$_{rms}$ when the dynamic biasing is off, and decreases to 80μV$_{rms}$ when the bias current is maximum. Figure 25.6.6 shows the filter frequency response for different blocker input levels. As seen, the activation of dynamic biasing does not significantly impact the filter in-band gain, the constancy of which is important for processing the desired signal.

The technique presented is useful for baseband channel filters, where large blockers are occasionally present and dictate the required linearity. It is also applicable to a variable IIP3 filter, where the linearity of the filter can be adjusted depending on the received signal profile, such as in the case of adaptive modulation reception.

Acknowledgement:
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References:

[1] 3GPP, "RF System Scenarios," 3G TR 25.942 2.1.3 (2000-03).
[2] N. Krishnapura and Y. Tsividis, "Noise and Power Reduction in Filters Through the Use of Adjustable Biasing," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1912-1020, Dec., 2001.
[3] M. Ozgun and Y. Tsividis, "Dynamically Power-Optimized Channel-Select Filter for Zero-IF GSM," *ISSCC Dig. Tech. Papers*, pp. 504-505, Feb., 2005.
[4] R. Hogervorst et al., "A Compact Power-Efficient 3V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries," *ISSCC Dig. Tech. Papers*, pp. 244-245, Feb., 1994.
[5] R. G. Meyer, "Low-Power Monolithic RF Peak Detector Analysis," *IEEE J. Solid-State Circuits*, vol. 30, no. 1, pp. 65-67, Jan., 1995.

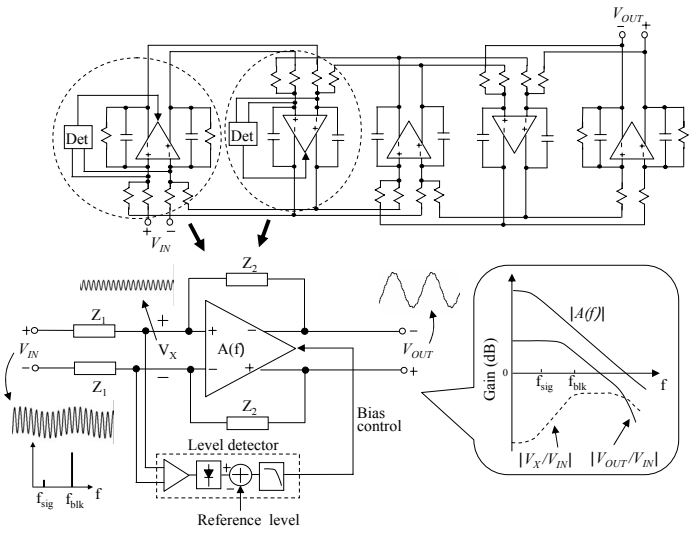

Figure 25.6.1: Proposed biasing technique in opamp *RC* filters.

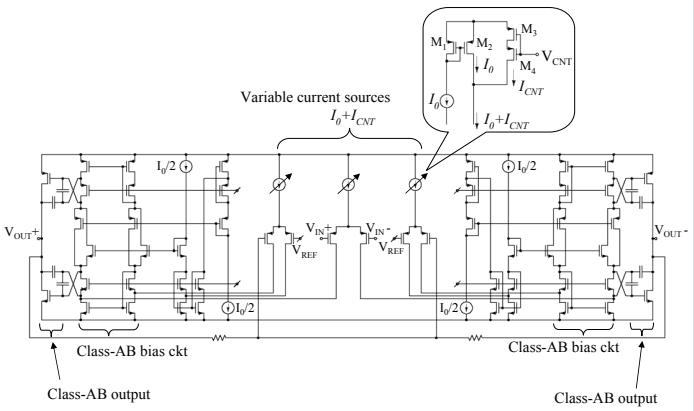

Figure 25.6.2: Fully differential class-AB output opamp with dynamic biasing.

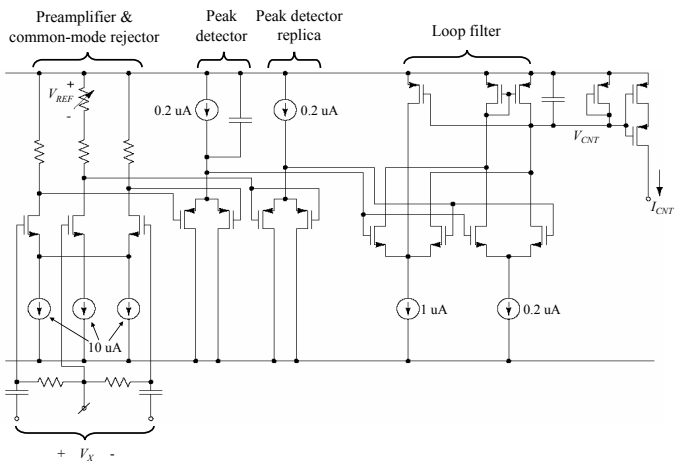

Figure 25.6.3: Level detector circuit.

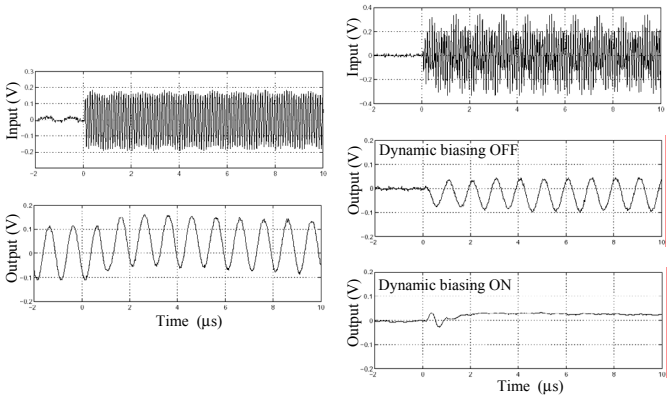

Figure 25.6.4: Transient response when a blocker appears the input at *t*=0.

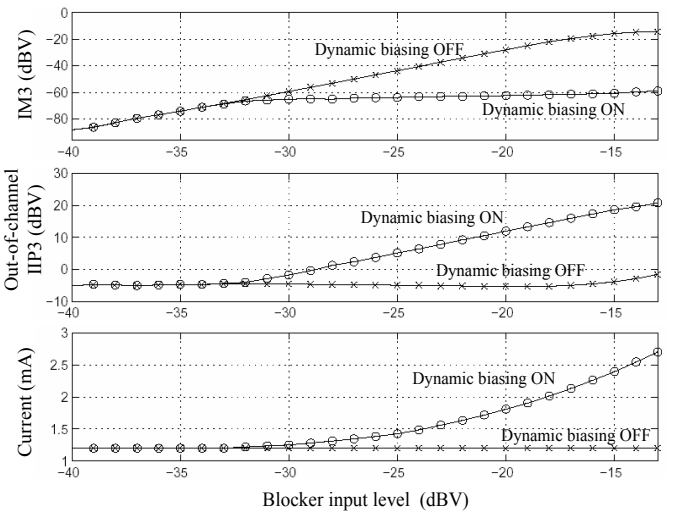

Figure 25.6.5: Filter IM3, instantaneous out-of-channel IIP3, and current consumption, versus blocker input level.

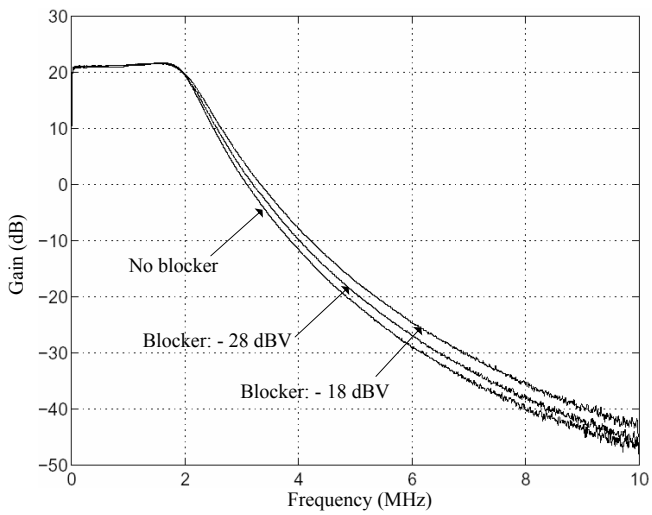

Figure 25.6.6: Measured filter frequency response for different blocker input levels.

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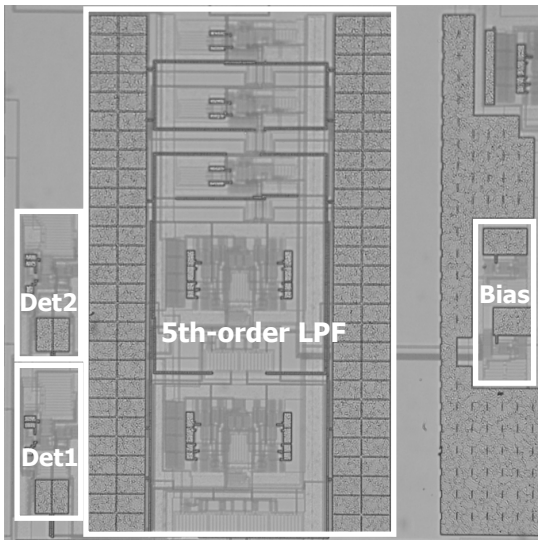

Figure 25.6.7: Chip micrograph.

